Fabrication and experimental demonstration of the first 160 Gb/s hybrid silicon-on-insulator integrated all-optical wavelength converter

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Abstract: We present a hybrid integrated photonic circuit on a silicon-on-insulator substrate that performs ultra high-speed all-optical wavelength conversion. The chip incorporates a 1.25 mm non-linear SOA mounted on the SOI board using gold-tin bumps as small as 14 μm. The device performs chirp filtering and signal polarity inversion with two multi-mode interference (MMI) - based cascaded delay interferometers (DIs) monolithically integrated on the same SOI substrate. Full free spectral range (FSR) tuning of the DIs is accomplished by two independently tuneable on-chip thermal heaters. We demonstrate 160Gb/s all-optical wavelength conversion with power penalties of less than 4.6dB.

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OCIS codes: (130.7405) Wavelength conversion devices; (130.3120) Integrated optics devices.

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1. Introduction

The complete range of data routing and signal processing functionalities continues to be the stronghold of electronics. However, the exponential network traffic growth is expected to impose a transformation in the shape of future routing hardware [1]. One of the main bottlenecks is the difficulty of electronic infrastructure to scale and support high-speed line-rates in a flexible, low-cost and energy-efficient way. The penetration of photonics in central offices hosting large sized equipment racks is already evident; router racks are now interconnected optically to reduce the massive amount of cumbersome electrical wiring. Apart from optical interconnections, photonic integrated solutions are also worked out to penetrate deeper into the heart of routing machines [2,3]. The development of scalable all-optical wavelength converters (AOWCs) with line-rate capacity beyond the one of electronics remains in the top priority of research on broadband photonic routing systems for the realization of wavelength division multiplexing (WDM) Tb/s switching fabrics.

So far a number of all-optical wavelength conversion techniques have been proposed suitable for photonic routing architectures. Four wave mixing in passive waveguides has enabled wavelength transparency at ultra-fast data rates but at the expense of high signal power levels [4]. Cross-gain modulation (XGM) or cross-phase modulation (XPM) in semiconductor optical amplifiers (SOAs) has been deployed in integrated interferometers but with performance limitations due to the SOA recovery lifetime [5]. This difficulty has recently been addressed with chirp filter assisted SOA schemes that perform phase-to-amplitude conversion using both XGM-XPM effects. A SOA-DI packaged and pigtailed device has been demonstrated in the past using monolithic integration in InP [6]. Bit rate performance >100 Gb/s has been attempted as well with discrete components consisting of SOAs followed by fiber pigtailed bulk filters [7], micro-ring resonators [8] or DI circuits [9].

The recent advances in silicon-on-insulator (SOI) photonic integration technology have enabled the development of fully integrated devices mainly for optical interconnects and data communications. Dense integration of passive components is combined with heterogeneous or hybrid integration of active components on-chip [10,11]. The III-V-on-SOI integration has demonstrated recently micro-disk lasers integrated on SOI nanowire substrates that can achieve wavelength conversion up to 10 Gb/s [10]. One promising solution to scale the bit-rates and avoid the nanowire waveguide and coupling losses, would be the hybridization of mature, pre-fabricated III-V components on micrometer SOI motherboards using microsolder bumps and flip-chip mounting [12].

In this paper we demonstrate the fabrication and experimental evaluation of the first reported hybrid SOI integrated AOWC. The photonic chip incorporates a 1.25 mm prefabricated non-linear SOA mounted on the SOI board using gold-tin bumps as small as 14 μm and with lateral placement misalignment <1μm. Optical filtering is realized by two cascaded delay interferometers (DIs) integrated as part of the SOI substrate using 2x2 multi-mode interference (MMI) couplers. The SOI waveguides are rib waveguides with a 4 μm height, 0.1 dB/cm waveguide and <0.5 dB coupling loss. Full free spectral range (FSR) tuning of the DIs is accomplished by two independently tuned on-chip thermal heaters. We demonstrate 160 Gb/s error-free wavelength conversion (WC) with power penalties < 4.6 dB and power consumption ~700mW.
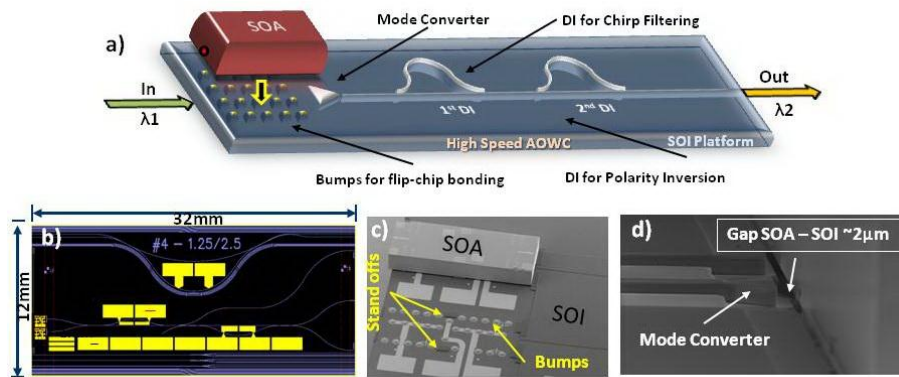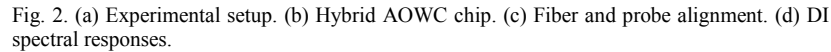
Fig. 1. (a) Layout of hybrid AOWC. (b) Mask design. (c) SEM image of SOA bonded on SOI. (d) SEM of SOA and SOI taper section.

2. Fabrication – SOI hybrid integration technology

Figure 1(a) depicts the layout of the hybrid SOI AOWC. The whole structure features two basic components: the SOA and the SOI integration board. The SOA is used as non linear element for wavelength conversion by means of cross gain and cross phase modulation effects. The SOI integration board performs wavelength processing with two cascaded delay interferometers. The first one is utilized as periodic WDM filter for chirp filtering and signal recovery time acceleration, whereas the second one as a notch filter for polarity inversion. Due to the periodicity of this comb-like filter structure, high-speed wavelength conversion is performed. Both SOA and SOI functionalities are combined in the same platform under the following procedure. A part of the SOI platform undergoes processing and bump deposition forming a landing site for the SOA which is flip-chip bonded on the SOI substrate, aligned to the SOI waveguide and mode matched through a tapered section.

The device development starts first with the fabrication of 1.25mm flip-chip adaptable SOAs with saturation power of 10dBm, a noise figure of 7dB, an internal single pass gain of 22dB (maximum value 25dB) and polarization sensitivity lower than 1.5dB. Besides the common requirements of in-line SOAs, additional challenges are associated with flip-chip compatibility. These include: i) adaption of the SOA output spot to the modal field of the SOI board waveguide, ii) high-precision optical alignment between SOA and SOI board waveguide, iii) enhanced metallization for reliable face-down interconnecting, and iv) imprint of identification data and alignment marks on the backside of the chip. For the current flip-chip adapted SOA design, a buried heterostructure with pn current blocking layers has been employed incorporating laterally tapered input/output waveguides serving as spot-size converters. For a proper horizontal and vertical optical alignment, alignment marks and dry etched trenches are implemented as counterparts to the board stand-offs. The interplay of these counterpart areas at the SOA chip with the stand-offs of the SOI board determines the vertical alignment, which is performed passively, whereas horizontal alignment is executed actively with a fine-placer via alignment marks.

The SOI board fabrication is a three step process: a) SOI waveguide etch and integration zone processing by etching through buried oxide and etching of alignment stands, b) complete metallization of SOI motherboard with electrical interconnects, Under Bump Metallization (UBM) and AuSn bump sputtering and c) back-end preparation of singled out motherboard dies with inspection and facet polishing. SOA flip-chip mounting into the SOI substrate has been performed by a high accuracy flip-chip bonder (1μm alignment precision) that takes over the positioning against the stand-offs and the thermal cycling for bump reflow and soldering. The reproducibility/uniformity of bump ball fabrication and the lift off the required post

Fig. 2. (a) Experimental setup. (b) Hybrid AOWC chip. (c) Fiber and probe alignment. (d) DI spectral responses.

processing (optimized reflow and soldering) has been achieved after a series of trial tests resulting to devices with proper mechanical stability and contact quality. Figure 1(b) depicts the developed SOI board mask layout with the SOA integration zone, the cascaded DIs and the heating elements. Figure 1(c) shows a close view of the SOI integration zone after bump deposition and metallization as well as the flip-chip bonded SOA on the SOI motherboard. Finally Fig. 1(d) presents the good horizontal and vertical alignment of the SOA facet with the SOI waveguide.

3. Device characterization

The fabricated AOWC board is depicted in Fig. 2(b) with the integrated SOA and the two DIs. The device was tested using the fiber and probe alignment station depicted in Fig. 2(c). A total of 6 electrical contacts were applied on the chip for driving the SOA and the DI heating elements. Optical fiber coupling was performed at the input of the SOA and at the waveguide facets of the double SOI Mach-Zehnder structure utilizing lensed fibers with 3μm spotsize diameter. The responses of the DIs were extracted using a tunable laser as seed and launch power of ~4dBm. Figure 2(d) illustrates the spectral response obtained after performing wavelength sweep with the tunable laser. The free-spectral-range (FSR) of the DIs has been measured 5.6nm and 2.52nm respectively and with proper wavelength tuning a spectral notch of ~30dB has been observed. The resistance of the heating elements has been calculated ~600Ωhm, the spectral efficiency ~6pm/mW and the maximum tuning range ~6nm. The bonded SOA was firstly inspected with SEM imaging showing proper integration, sufficient bump solder height and mechanical alignment in the range of μm. Then it was electrically biased up to 180mA (Voltage = 2.3V) revealing good electrical contact quality as well. The device temperature was maintained during measurements at 20°C using a thermo-electric cooler (TEC). Pump probe measurements were subsequently performed in order to assess the SOA recovery time. The output of a 10G mode-locked laser (pump signal) was combined with a continuous wave (CW) probe signal before injected into the AOWC. The SOA recovery time (Δt_{10-90}) was measured ~30ps with the DI responses aligned with the probe signal. The effective recovery time was measured <2ps with DI detuning. The losses from fiber coupling and DI detuning were compensated using an erbium-doped amplifier (EDFA) while the pump rejection was achieved with an additional filtering element. The significant rise-time reduction (below 1/3 of the 160Gb/s bit slot) was adequate for high-speed signal processing using the SOI AOWC chip. Typical gain figures of the SOA were around 20dB with weak polarization dependence. The output power of the chip for 4dBm optical input was ~0dBm showing proper x-y-z alignment between the SOA facet and the SOI waveguide.
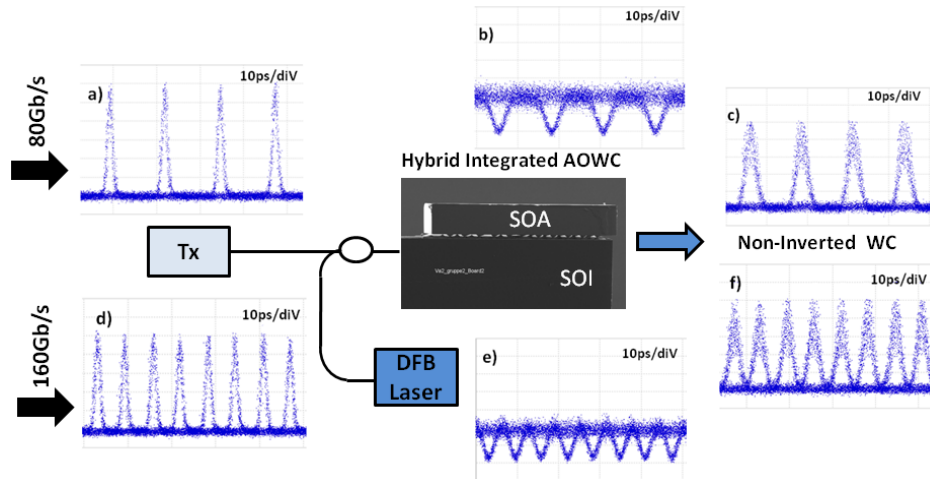
Fig. 3. Eye diagrams. (a-c) 80Gb/s B2B, Inverted WC, Non-Inverted WC. (d-f) 160Gb/s B2B, Inverted WC, Non-Inverted WC.

4. Experimental setup

Figure 2(a) shows the setup for the 160 Gb/s experiment. It comprises three main blocks: the 160 Gb/s optical transmitter, the SOA-DI wavelength converter and the evaluation stage. In the transmitter, optical pulses were generated by a mode-locked laser (MLL) at 1552 nm with duration of 2.2 ps and 10 GHz repetition rate. The pulses were encoded with a 2^7-1 PRBS using a LiNbO$_3$ modulator, compressed down to 440fs using 220m of high non-linear fiber (HNLF) with -0.25 ps/nm/km dispersion and 11.5 W^{-1}km^{-1} non-linear parameter and time-multiplexed through fiber interleavers in order to constitute the 160Gb/s data stream (pump signal). The generated data sequence was combined then with the output of a distributed-feedback (DFB) laser diode at 1542nm (probe signal) before being injected into the hybrid integrated AOWC through lensed fibers. The incoming data sequence was interacting into the SOA with the DFB output resulting to inverted wavelength conversion via cross-gain modulation (XGM). The cross-phase modulation (XPM) was producing subsequently a chirped wavelength converted signal with red-shifted leading edges and blue-shifted trailing edges. The first DI element was employed for selecting the blue-shifted sideband of the wavelength converted signal accelerating significantly its recovery time. The second DI was operating then as a notch filter for carrier frequency suppression and signal polarity inversion. Wavelength spectral tuning for both the DIs was achieved using the integrated heating elements.

At the receiver side the wavelength converted signal was evaluated after performing a two-stage optical demultiplexing. The output of the AOWC was amplified first by an EDFA, pump signal was rejected employing a 4nm Gaussian filter and the converted signal was subsequently demultiplexed to 40Gb/s using a non-linear loop mirror (NOLM). The non-linear element of the NOLM was 100m of HNLF with 10 W^{-1}km^{-1} non linear parameter and 1.21 ps/nm/km dispersion. As control signal into the NOLM, a mode-locked laser at 1553nm was utilized emitting 1.3ps optical pulses at 40GHz repetition rate. The output of the NOLM, after filtering the control signal, was eventually directed to an electro-absorption modulator (EAM) for optical demultiplexing to 10Gb/s. The hybrid integrated wavelength converter was experimentally tested for data rates at 80Gb/s and 160Gb/s. In both cases the SOA was driven with 180mA, temperature was maintained at 20°C, while the detuning of the DIs with respect to the probe wavelength carrier was 0.8nm and 1.3nm respectively. The average optical power for the probe signal was 8dBm, for the 80Gb/s pump signal 10dBm and for the 160Gb/s pump ~12dBm. Power levels were measured at the input pigtail of the lensed fiber.
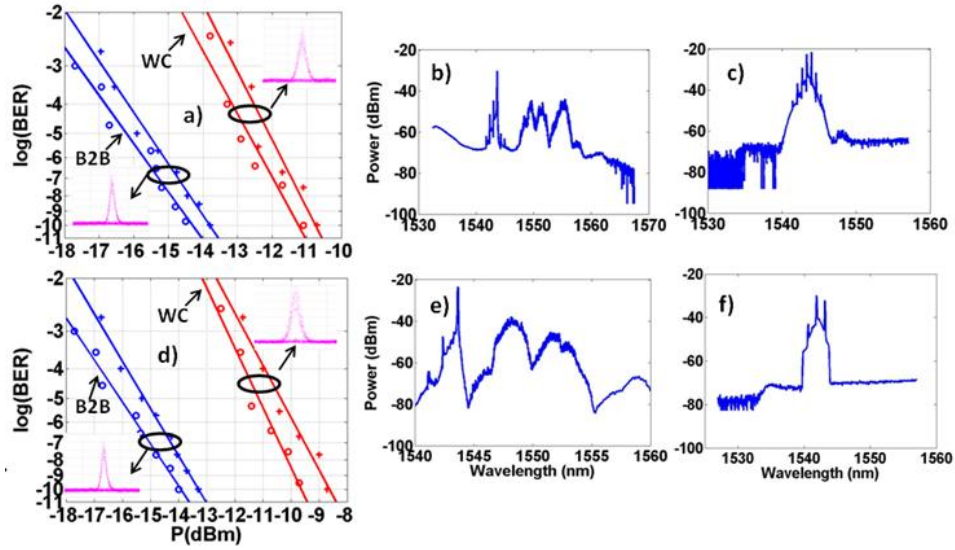
Fig. 4. (a) BER curves of 80Gb/s WC. (b) Output spectrum of AOWC at 80Gb/s. (c) Spectrum of 80Gb/s Nov-Inverted WC. (d) BER curves of 160Gb/s WC. (e) Output spectrum of AOWC at 160Gb/s. (f) Spectrum of 160Gb/s Nov-Inverted WC.

5. Experimental results

Figure 3 depicts the high-speed measurements performed with the hybrid integrated AOWC. Figures 3(a) and 3(d) show the eye-diagrams of the incoming 80Gb/s and 160Gb/s data streams that were injected into the SOA for cross gain and phase modulation. The slight amplitude variation observed between the pulses was attributed to the non-optimum equalization in the fiber-interleaver. After spectral detuning the DIs off the probe carrier, the wavelength converted signals of Fig. 3(b) and 3(e) were obtained. Although the waveforms were on inverted mode, a clear open pattern was evident indicating that chirp-filtering and signal recovery acceleration were successfully performed with the on-board SOI filtering elements. Figures 3(c) and 3(f) depict the non-inverted wavelength converted signals when placing the probe signal in a filter notch generated by tuning and overlapping two subsequent DI filter dips. The signal polarity was effectively restored for both data rates (80 and 160Gb/s). The output power obtained at the chip output was lower in the case of 160 Gb/s due to the larger DI detuning. In more detail for 80Gb/s operation the power after the hybrid AOWC was −12dBm and after post amplification and pump rejection the wavelength converted signal had a signal-to-noise ratio (SNR) of 25dB. For 160Gb/s operation the power level after the AOWC was −15dBm while the final wavelength converted signal had a SNR of 19dB. This explains the increased amplitude noise shown in Fig. 3(f) with respect to Fig. 3(c). Furthermore the pulse broadening experienced after the hybrid integrated AOWC, was mainly attributed to the narrow bandwidth of the integrated DIs as well as to the narrow filtering elements used (~5nm) for pump rejection and amplification.

Figure 4 depicts the bit-error-rate measurements for 80Gb/s and 160Gb/s wavelength conversion as well as the spectrum traces recorded at the AOWC output. Error free operation was achieved for all the demultiplexed channels at 80Gb/s with power penalties less than 3.2dB. We present the best and worst channel performance in Fig. 4(a). Figure 4(b) shows the 80Gb/s wavelength converted signal spectral shape, when slight offset filtering is applied. In the same figure the spectrum of the pump data stream, the combined response of the cascaded DI structures as well as the dominant carrier component resulting to an inverted version of the wavelength converted signal are observed. In order to obtain a non-inverted waveform, it was necessary one of the DI notches to coincide with the probe wavelength either by assigning the

correct wavelength to the DFB laser or by thermally tuning the DI responses. This was successfully implemented as shown in Fig. 4(c). Figure 4(d) illustrates the BER curves for the 160Gb/s wavelength conversion. Error-free operation has been achieved for all the demultiplexed channels with power penalties ~4.6dB. The higher penalty value was attributed to the smaller AOWC output power which yields a higher OSNR degradation following signal post-amplification. An improved wavelength conversion performance is expected in the next generation devices due to a better alignment between SOA facet and SOI waveguide that will minimize losses. Figures 4(e) and 4(f) depict the spectrum traces of the final 160Gb/s inverted and non-inverted converted signals after DI offset filtering and probe carrier suppression respectively.

6. Conclusion

We have fabricated and system tested for the first time a hybrid all-optical wavelength converter integrated on a SOI substrate. The photonic chip performs inverted and non-inverted wavelength conversion up to 160Gb/s using a flip-chip mounted SOA and two concatenated SOI DIs. Error-free operation has been accomplished with power penalties less than 4.6dB.

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